

What is claimed is:

- 1 1. An apparatus comprising:
2 a first processor that includes a first processor element; and
3 a second processor that includes a second processor element, wherein the
4 first processor is configured to transmit data to the second processor through a third
5 processor, wherein no processor element within the third processor is configured to
6 perform a process operation on the data as part of the transmission of the data from
7 the first processor to the second processor.
- 1 2. The apparatus of claim 1, wherein the first processor is not directly
2 connected with the second processor.
- 1 3. The apparatus of claim 1, wherein no processor element within the third
2 processor is involved in the transmission of data from the first processor to the
3 second processor through the third processor.
- 1 4. The apparatus of claim 1, wherein the first processor, the second processor
2 and the third processor are coupled together in a point-to-point configuration.
- 1 5. An apparatus comprising:
2 a first processor that includes a first processor element that is configured to
3 perform a first data process operation; and
4 a second processor that includes a second processor element that is
5 configured to perform a second data process operation based on an output from the
6 first data process operation, the first processor to transmit the output from the first
7 data process operation to the second processor based on a logical connection that
8 includes traversal through a port ring of a third processor, wherein a third processor
9 element within the third processor is not configured to perform a data process

10 operation between the first data process operation and the second data process
11 operation.

1 6. The apparatus of claim 5, wherein the first processor, the second processor
2 and the third processor are part of a number of processors that are in a point-to-point
3 configuration.

1 7. The apparatus of claim 5, wherein the first processor includes a type of
2 hardware accelerator that is not included in the second processor.

1 8. The apparatus of claim 5 further comprising,
2 an expansion interface to receive data on which the processor element in the
3 first processor is to perform the first data process operation; and
4 a memory interface unit coupled to a memory that is external to the
5 apparatus, wherein the memory is configured to store an output of the second data
6 process operation.

1 9. The apparatus of claim 8, wherein the first processor element in the first
2 processor is configured to perform the first data process operation on data streams
3 received into the expansion interface at least simultaneously in part with second data
4 process operation performed by the second processor element in the second
5 processor.

1 10. An apparatus comprising:
2 a number of image signal processors having a number of ports that couple
3 the number of image signal processors together in a point-to-point configuration,
4 wherein at least one of the number of image signal processors includes a number of
5 processor elements and a hardware accelerator; and
6 an expansion interface to receive data into the apparatus to be processed by
7 the number of image signal processors.

1 11. The apparatus of claim 10, wherein a processor element within a source
2 image signal processor of the number of image signal processors is to output a result
3 of an image process operation to a destination image signal processor of the number
4 of image signal processors.

1 12. The apparatus of claim 11, wherein the processor element within the source
2 image signal processor is configured to output the result of the image process
3 operation to the destination image signal processor through a logical connection that
4 includes a port of an intermediate image signal processor of the number of image
5 signal processors, wherein no processor elements in the intermediate image signal
6 processor are configured to process the result of the image process operation prior to
7 receipt by the destination image signal processor.

1 13. The apparatus of claim 10 further comprising a bus coupled to communicate
2 configuration data to the number of image signal processors, wherein the bus is
3 independent of the point-to-point configuration.

1 14. The apparatus of claim 13, wherein the configuration data includes data to
2 establish logical connections between the number of image signal processors.

1 15. A system comprising:
2 a Charge Coupled Device (CCD) sensor to capture an image;
3 an image processor that includes a number of processors coupled together in
4 a point-to-point configuration, the number of processors to include a number of
5 processor elements, wherein the number of processor elements are to process the
6 image based on one of a number of image process operations;
7 a memory to store at least one output of the execution of the number of
8 image process operations by the number of processor elements; and

9 a host processor to configure the execution of the number of image process
10 operations within the image processor.

1 16. The system of claim 15, wherein the image processor includes a global bus
2 that is coupled to the number of processors, the global bus independent of the point-
3 to-point connections among the number of processors.

1 17. The system of claim 16, wherein the host processor is configured to transmit
2 configuration data to the number of processors for generation of a logical
3 connection, wherein the logical connection from a source processor to a destination
4 processor includes connection paths among at least a part of the number of
5 processors to process the image based on the number of image process operations.

1 18. The system of claim 17, wherein the processor elements within the at least
2 part of the number of processors within the logical connection are not involved in
3 the transmission of data from the source processor to the destination processor.

1 19. A method comprising:
2 receiving a stream of data in a first processor having a first processor
3 element;
4 performing, by the first processor element, image processing operations on
5 at least a part of the stream of data; and
6 transmitting a result of the image processing operations to a second
7 processor through a third processor having a third processor element, independent of
8 image processing operations by the third processor element.

1 20. The method of claim 19, wherein transmitting the result of the image
2 processing operations to the second processor through the third processor includes
3 transmitting the result of the image processing operations to the second processor

4 through a logical connection that includes transmission through a series of
5 processors including the third processor.

1 21. The method of claim 19, wherein receiving the stream of data in the first
2 processor having the first processor element includes receiving the stream of data in
3 the first processor having the first processor element at least simultaneously in part
4 with performing, by a second processor element in the second processor, a different
5 image processing operation.

1 22. A method comprising:
2 performing, by a first image signal processor within a multi-processor point-
3 to-point configuration, the following operations until receipt of image data from an
4 image scanning operation is complete,
5 executing, by a first processor element in the first image signal
6 processor, an image process operation on the image data; and
7 transmitting a result of the image process operation to a second
8 image signal processor within the multi-processor point-to-point configuration
9 through a logical connection that includes a number of ports of a number of other
10 different image signal processors within the multi-processor point-to-point
11 configuration.

1 23. The method of claim 22, wherein transmitting the result of the image process
2 operation to the second image signal processor includes transmitting the result of the
3 image process operation to the second image signal processor through the logical
4 connection, wherein other processing elements in the other different image signal
5 processors do not process the image data prior to processing by a second processor
6 element in the second image signal processor.

1 24. The method of claim 22 further comprising receiving the image data from a
2 source that is external to the multi-processor point-to-point configuration.

1 25. A machine-readable medium that provides instructions, which when
2 executed by a machine, cause said machine to perform operations comprising:
3 receiving a stream of data in a first processor having a first processor
4 element;
5 performing, by the first processor element, image processing operations on
6 at least a part of the stream of data; and
7 transmitting a result of the image processing operations to a second
8 processor through a third processor having a third processor element, independent of
9 image processing operations by the third processor element.

1 26. The machine-readable medium of claim 25, wherein transmitting the result
2 of the image processing operations to the second processor through the third
3 processor includes transmitting the result of the image processing operations to the
4 second processor through a logical connection that includes transmission through a
5 series of processors including the third processor.

1 27. The machine-readable medium of claim 25, wherein receiving the stream of
2 data in the first processor having the first processor element includes receiving the
3 stream of data in the first processor having the first processor element at least
4 simultaneously in part with performing, by a second processor element in the
5 second processor, a different image processing operation.

1 28. A machine-readable medium that provides instructions, which when
2 executed by a machine, cause said machine to perform operations comprising:
3 recursively performing, by a first image signal processor within a multi-
4 processor point-to-point configuration, the following operations until receipt of
5 image data from an image scanning operation is complete,
6 executing, by a first processor element in the first image signal processor, an
7 image process operation on the image data; and

8 transmitting a result of the image process operation to a second image signal
9 processor within the multi-processor point-to-point configuration through a logical
10 connection that includes a number of ports of a number of other different image
11 signal processors within the multi-processor point-to-point configuration.

1 29. The machine-readable medium of claim 28, wherein transmitting the result
2 of the image process operation to the second image signal processor includes
3 transmitting the result of the image process operation to the second image signal
4 processor through the logical connection, wherein other processing elements in the
5 other different image signal processors do not process the image data prior to
6 processing by a second processor element in the second image signal processor.

1 30. The machine-readable medium of claim 28 further comprising receiving the
2 image data from a source that is external to the multi-processor point-to-point
3 configuration.